REMARKS

Claims 1-22 remain in the present application. Independent Claims 1, 9, and 17 have been amended. Reconsideration of this application is respectfully requested in light of the above amendments and the remarks below.

35 U.S.C. Section 102 Rejections

Paragraphs 1 and 2 of the above referenced Office Action state that Claims 1, 3, and 9 are rejected under 35 U.S.C. Section 102(b) as being anticipated by Waits, U.S. Patent No. 3,649,945 (hereafter Waits). Applicants have herein amended the independent claims to more particularly point out aspects of the claimed invention. Accordingly, Applicants respectfully submit that the present invention as recited in independent Claims 1, 9, and 17 is not anticipated by Waits.

Specifically, Claim 1 has been amended to recite a method for making a resistive heater for a planar lightwave circuit, including the step of "depositing an interconnect layer onto the resistive layer" (emphasis added). Applicants point out that the claimed embodiments deposit the interconnect layer directly onto the resistive layer. This is shown in the embodiment depicted in, for example, Figure 6 of the specification of the present application, where an interconnect layer (e.g., aluminum 602) is deposited onto a resistive layer (e.g., tungsten 601).

In contrast, Waits explicitly shows and teaches an interconnect layer not being deposited on the resistive layer. For example, Figure 1 of Waits shows the resistive layer (resistive film 10) separated from the interconnect layer (aluminum 18) by an intermediate layer (molybdenum 16). In other words, the interconnect layer is not deposited onto the resistive layer as explicitly stated in Claim 1.

Accordingly, Applicants respectfully assert that the present invention as recited in amended Claim 1 is not anticipated by the Waits reference. Independent Claims 9 and 17 have been similarly amended to recite an interconnect layer deposited onto a resistive layer. Thus, Claims 1-22 are not anticipated by Waits within the meaning of 35 U.S.C. Section 102.

Paragraph 3 of the above referenced Office Action states that Claims 1-4, 7-10, 12, 15-18, and 20-22 are rejected under 35 U.S.C. Section 102(a) as being anticipated by Xu, et al., U.S. Patent No. 2002/0075346 A1 (hereafter Xu). Applicants respectfully submit that the present invention as recited in independent Claims 1, 9, and 17 is not anticipated by Xu.

Specifically, Claim 1 recites the step of depositing a resistive layer on a top clad of a planar lightwave circuit. Applicants point out that Xu does not show or teach a top clad. Xu does not disclose or teach a planar lightwave circuit. These limitations are included in independent Claims 9 and 17. Accordingly, the present invention as recited in independent Claims 1, 9, and 17 is not anticipated by Xu within the meaning of 35 U.S.C. Section 102.

35 U.S.C. Section 103 Rejections

Paragraph 5 states that Claims 5-6, 11, 13-14, and 19 are rejected under 35 U.S.C. Section 103(a) as being unpatentable over Xu, in view of Bischel et al., U.S. Patent No. 2002/0018636 A1 (hereafter Bischel). Applicants respectfully traverse.

Applicants submit that the addition of Bischel does not cure the defects of Xu. The cited combination does not show depositing a resistive layer on a top clad of a planar lightwave circuit and depositing an interconnect layer onto the resistive layer, as recited in, for example Claim 1 of the present application (emphasis added). These limitations are similarly recited in independent Claims 9 and 17. Accordingly, Applicants submit that the present invention is not rendered unpatentable by the cited combination within the meaning of 35 U.S.C. Section 103.

CONCLUSION

In view of the above amendments and remarks, Applicants respectfully assert that all claims of the present application are now in condition for allowance, and such action is earnestly solicited.

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present application. Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,
WAGNER, MURABITO & HAO

Dated: 1/21, 2003

Glenn Barnes
Registration No. 42,293

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A method for making a resistive heater for a planar lightwave circuit, the method comprising the steps of:

a) depositing a resistive layer on a top clad of a planar lightwave circuit;

b) depositing an interconnect layer [over] onto the resistive layer;

c) etching the interconnect layer to define a heater interconnect, wherein the heater interconnect is disposed over the resistive layer and has a first width;

d) masking the heater interconnect; and

e) etching the resistive layer to define a resistive heater, wherein the resistive heater is disposed beneath the heater interconnect and has a second width larger than the first width.

9. (Amended) A method for making a resistive heater for an active planar lightwave circuit, the method comprising the steps of:

a) depositing a tungsten resistive layer on a top clad of a planar lightwave circuit;

b) depositing an aluminum interconnect layer [over] onto the resistive layer such that the tungsten resistive layer functions as an adhesion layer for the aluminum interconnect layer;

c) etching the aluminum interconnect layer to define a heater interconnect, wherein the heater interconnect is disposed over the tungsten resistive layer and has a first width;

d) masking the heater interconnect; and

e) etching the tungsten resistive layer to define a resistive heater, wherein the resistive heater is disposed beneath the heater interconnect and has a second width larger than the first width.

17. (Amended) A method for making a thermo-optic resistive heater for an active planar lightwave circuit, the method comprising the steps of:

a) depositing a tungsten layer on a top clad of a planar lightwave circuit;

b) depositing an aluminum layer [over] <u>onto</u> the tungsten layer such that the tungsten layer functions as an adhesion layer for the aluminum layer;

c) masking a region of the aluminum layer to be subsequently defined as a heater interconnect;

d) etching the aluminum layer to define the heater interconnect, wherein the heater interconnect is disposed over the tungsten layer and has a first width;

e) masking the heater interconnect and masking a region of the tungsten layer to be subsequently defined as a resistive heater; and

f) etching the tungsten resistive layer to define the resistive heater, wherein the resistive heater is disposed beneath the heater interconnect and has a second width larger than the first width.